## REMARKS

Favorable reconsideration of this application is respectfully requested in view of the following remarks. Claims 14-27 are pending in the present application, of which Claims 14, 25 and 27 are independent. Claims 1-13 have been cancelled without prejudice or disclaimer of the subject matter contained therein. Claims 20-27 have been added. No new matter has been introduced by way of the claim additions and entry thereof is respectfully requested.

*Election/Restriction*

The Official Action acknowledges that Applicant wishes to revive and prosecute the previously cancelled Claims 14-19. As noted in Applicant's November 17, 2004 response to a restriction requirement, the preliminary amendment filed on October 22, 2003 incorrectly requested the cancellation of Claims 14-19. The preliminary amendment should have requested the cancellation of Claims 1-13, as Claims 1-13 were elected in the parent application. The withdrawal of Claims 1-13 and the examination of Claims 14-19 in the Official Action is noted with appreciation.

*Drawings*

The Official Action does not indicate whether the drawings filed on October 22, 2003 are approved. Applicant respectfully requests approval of the original filed drawings.

*Specification*

The title has been amended to more accurately reflect the subject matter of the present application. Entry of the amendment to the title is respectfully requested.

*Claim Rejection under 35 U.S.C. 102*

The test for determining if a reference anticipates a claim, for purposes of a rejection under 35 U.S.C. § 102, is whether the reference discloses all the elements of the claimed combination, or the mechanical equivalents thereof functioning in substantially the same way to produce substantially the same results. As noted by the Court of Appeals for the Federal Circuit in *Lindemann Maschinenfabrick GmbH v. American Hoist and Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984), in evaluating the sufficiency of an anticipation rejection under 35 U.S.C. § 102, the Court stated:

> Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim.

Therefore, if the cited reference does not disclose each and every element of the claimed invention, then the cited reference fails to anticipate the claimed invention and, thus, the claimed invention is distinguishable over the cited reference.

Rejection of Claims 14-19 under 35 U.S.C. § 102(e)

The Official Action sets forth a rejection of claims 14-19 under 35 USC 102(e) as allegedly being anticipated by U.S. Patent No. 6,617,206 to Sandhu et al. ("Sandhu et al."). This rejection is respectfully traversed.

Sandhu et al. discloses a capacitor structure for a dynamic random access memory (DRAM) array (Column 3, lines 65 through Column 4, lines 1-5; Abstract). According to Sandhu et al., a dielectric is deposited in a series of thin layers and oxidized in a series of oxidation steps, as opposed to a depositing of a single thick layer. (Abstract).

Claim 14 recites an on-chip by-pass capacitor, comprising "a first electrode formed during a deposition of a first metal layer of a multi-level deposition device," "a substantially

thin dielectric layer configured to be deposited over said first electrode" and "a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer."

Sandhu et al. fails to teach "a first electrode formed during a deposition of a first metal layer of a multi-level deposition device," as recited in claim 14. The Official Action refers to Figure 2A, reference numeral 20, and alleges that Sandhu et al. discloses an on-chip by-pass capacitor comprising a first electrode formed during a deposition of a first metal layer of a multi-level deposition device. However, the Official Action appears to be unsupported by the disclosure of Sandhu et al. Specifically, reference numeral 20 in Figure 2A of Sandhu et al. corresponds to a conductive layer 20 (Column 4, lines 63-67). Sandhu et al. fails to teach that the conductive layer 20 of the DRAM substrate assembly 10A constitutes "a first electrode formed during a deposition of a first metal layer of a multi-level deposition device." Instead, Sandhu et al. discloses that the conductive layer 20 provides an electrode for a container capacitor structure (Column 4, lines 18-21) and that the conductive layer 20 is formed as part of "an *in-process* DRAM substrate assembly 10A" (Figure 2A; Column 4, lines 63-67). In addition, Sandhu et al. discloses that the conductive layer 20 is formed after the deposition of a plurality of non-conductive and conductive layers. Specifically, Sandhu et al. discloses that

> Substrate assembly 10 comprises a slice of a single crystalline semiconductor 11. In semiconductor 11, a well 12 is formed. In well 12 are formed conductive implant regions 14. Transistor gate stacks 16 are formed on semiconductor 11, and are separated from conductive studs 15 by spacers 17. Dielectric layers 18 and 19 are deposited and etched to provide holes for deposition of conductive layer 20. (Column 3, lines 42-52; Figure 1A)

Thus, according to Sandhu et al., the conductive layer 20 *is formed after, and not during*, the deposition of a plurality of non-conductive and conductive layers, including the

transistor gate stacks 16 and the conductive studs 15. Even assuming that the DRAM substrate assembly 10A were a multi-level deposition device, which Sandhu et al. fails to teach, the above-cited passage clearly indicates that conductive layer 20 fails to constitute "a first electrode formed during a deposition of a first metal layer of a multi-level deposition device" (emphasis added). Given that the transistor gate stacks 16 and the conductive studs 15 are deposited and formed prior to the deposition of the conductive layer 20, the conductive layer 20 must necessarily be formed after, and not during, a deposition of a first metal layer of the DRAM substrate assembly 10A. Sandhu et al. thus fails to teach that the conductive layer 20 constitutes a first electrode "formed during a deposition of a first metal layer of a multi-level deposition device."

The Official Action also refers to reference numeral 24 of Figure 2A, and also cites Column 5, lines 50-55, as evidence that Sandhu et al. discloses "a substantially thin dielectric layer configured to be deposited over said first electrode." It appears the Official Action is alleging that reference numeral 24 of Figure 2A constitutes "a substantially thin dielectric layer configured to be deposited over said first electrode." However, Sandhu et al. fails to teach that reference numeral 24 of Figure 2A constitutes a substantially thin dielectric layer. Instead, Sandhu et al. discloses providing "two or more sub-layers for forming capacitor dielectric layer 24" (Column 7, lines 34-36). Sandhu et al. also discloses "repetitively forming sub-layers of capacitor dielectric 24" and "forming a plurality of sub-layers of capacitor dielectric 24" (Column 7, lines 9-10 and lines 22-23). In addition, in the passage corresponding to Column 5, lines 50-55, as cited by the Official Action, Sandhu et al. fails to teach a substantially thin dielectric layer, but instead discloses a CVD process that involves a tantalum precursor.

The Official Action also refers to reference numeral 25 of Figure 3B, and alleges that Sandhu et al. discloses "a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer." However, this rejection appears to be unsupported by the disclosure of Sandhu et al. Specifically, as noted above, Sandhu et al. discloses a plurality of conductive layers, including the conductive layers that form the transistor gate stacks 16 and the conductive studs 15, that are formed prior to formation of the layer 25 (Column 3, lines 42-52; Figures 1A and 3B). Given that the transistor gate stacks 16, the conductive studs 15 and the conductive layer 20 are deposited and formed prior to the deposition of the layer 25, the layer 25 must necessarily be formed after, and not during, a deposition of a second metal layer of the DRAM substrate assembly 10B. Sandhu et al. thus fails to teach "a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer." For at least the same reasons, Sandhu et al. fails to teach the features as recited in independent Claim 14.

Because Claims 15-19 incorporate all the features of Claim 14, Sandhu et al. fails to teach the invention claimed in Claims 15-19 for at least the reasons given above. Therefore, for at least the reasons set forth above, Sandhu et al. does not anticipate the subject matter of Claims 14-19. Claims 14-19 are thus allowable over Sandhu et al., and withdrawal of the rejection is respectfully requested.

*Newly Added Claims*

Claims 20-27 have been added. Claims 20-24 each depend from allowable Claim 14 and are also allowable at least by virtue of their dependencies. Claim 25 recites "a first electrode," "a substantially thin dielectric layer," "a second electrode" and "at least one via between the second electrode and the substantially thin dielectric layer." Claim 26 incorporates all the features of Claim 25, and in addition recites "two barrier layers, wherein the substantially thin dielectric layer is positioned between the two barrier layers." Claim 27 recites "a first electrode formed during a deposition of a first metal layer of a multi-level deposition device," "a substantially thin dielectric layer configured to be deposited over said first electrode," "a second electrode formed during a deposition of a second metal layer of said multi-level deposition device, wherein said second electrode is formed over said substantially thin dielectric layer," "at least one via between the second electrode and the substantially thin dielectric layer" and "two barrier layers, wherein the substantially thin dielectric layer is positioned between the two barrier layers." Claims 25-27 are not taught or suggested by the prior art for at least those reasons set forth above with respect to Claim 14. Therefore, the Examiner is respectfully requested to also allow Claims 20-27.

*Conclusion*

In light of the foregoing, withdrawal of the rejections of record and allowance of this application are earnestly solicited.

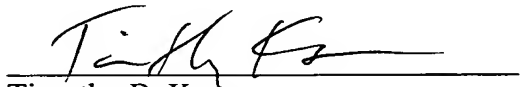
Should the Examiner believe that a telephone conference with the undersigned would assist in resolving any issues pertaining to the allowability of the above-identified application, please contact the undersigned at the telephone number listed below.

Please grant any required extensions of time and charge any fees due in connection with this request to deposit account no. 08-2025.

Respectfully submitted,

Osamu Samuel Nakagawa

Dated: March 11, 2005

By 

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